AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An ~~apparatus, apparatus~~ comprising:

a variable speed bus; the variable speed bus initialized with a first clock frequency;

a first unit coupled to the variable speed bus, the first unit having a first rate of requests to access the variable speed bus;

a second unit coupled to the variable speed bus, the second unit having a second rate of requests to access the variable speed bus; and

an arbitration and bus clock control unit to monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on at least one of the first access rate and the second access request rate, wherein the arbitration and bus clock control unit to track a rate of request of the first and second units to access the variable speed bus, the arbitration and bus clock control unit is further to instruct a clock throttling logic to adjust a clock frequency associated with the variable speed bus according to bandwidth requirements of the first and second units based on the rate of request.

2. (Currently Amended) The apparatus of claim 1, wherein the first unit ~~is~~ comprises a processor unit.

3. (Currently Amended) The apparatus of claim 1, wherein the second unit ~~is~~ comprises a video processor unit.

4. (Currently Amended) The apparatus of claim 1, wherein the first unit ~~is~~ comprises a hard disk drive controller unit.

5. (Currently Amended) The apparatus of claim 1, wherein the second unit ~~is~~ comprises an isochronous data transfer unit.

6. (Cancelled)

7. (Currently Amended) The apparatus of claim 5, wherein the isochronous data transfer unit ~~is~~ comprises a 1394 controller unit.

8. (Currently Amended) The apparatus of claim 5, wherein the isochronous data transfer unit ~~is~~ comprises a USB controller unit.

9. (Cancelled)

10. (Currently Amended) A ~~system, system~~ comprising:

a device coupled to a variable speed bus, the device having a rate of request to access the variable speed bus; and

an arbitration and bus clock control unit to monitor the rate of request, and to determine a clock frequency associated with the variable speed bus based on the rate of request, wherein the arbitration and bus clock control unit to track the rate of request to access the variable speed bus, the arbitration and bus clock control unit is further to instruct a clock throttling logic to adjust ~~a~~ the clock frequency associated with the variable speed bus based on the rate of request to access the variable speed bus from the device.

11. (Cancelled)

12. (Currently Amended) The system of claim 10, wherein the device coupled to the variable speed bus ~~is~~ comprises a processor.

13. (Currently Amended) The system of claim 10, wherein the device coupled to the variable speed bus ~~is~~ comprises a video processor.

14. (Currently Amended) The system of claim 10, wherein the device coupled to the variable speed bus ~~is~~ comprises a hard disk drive controller.

15. (Currently Amended) The system of claim 10, wherein the device coupled to the variable speed bus ~~is~~ comprises an isochronous data transfer controller.

16. (Cancelled)

17. (Currently Amended) The system of claim 15, wherein the isochronous data transfer controller ~~is~~ comprises a 1394 controller.

18. (Currently Amended) The system of claim 15, wherein the isochronous data transfer controller ~~is~~ comprises a USB controller.

19-21 (Cancelled)

22. (Previously Presented) The apparatus of claim 21, wherein the arbitration and bus clock control unit determines the second clock frequency based on a first bandwidth requirement from the first unit and a second bandwidth requirement from the second unit, the first bandwidth requirement derived from the first rate of request to access the variable speed bus from the first unit, the second bandwidth requirement derived from the second rate of request to access the variable speed bus from the second unit.

23. (Previously Presented) The apparatus of claim 21, wherein the variable speed bus, the first unit, the second unit, the clock throttling logic and the arbitration and clock control unit are located on a single semiconductor die.

24. (Cancelled)